PHASE DECREMENT TYPE DIRECT FREQUENCY SYNTHSIZER DRIVEN BY A DDS

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***Abstract* — A phase decrement type direct frequency synthesizer with a quadrature mixer driven by a DDS is presented. Phase decrement of a DDS signal can increase bandwidth of the direct synthesizer. Overflow of a DDS is employed to achieve phase decrement of the signal without adding an extra circuit. A developed 2GHz-band synthesizer with sub Hz order frequency step that achieves 240MHz bandwidth, frequency switching time of less than 2μs, phase noise of –117dBc/Hz at 100kHz offset, and consumption current of 685mA.**

I. INTRODUCTION

In digital mobile radio transmission systems [1]-[2], requirements of frequency synthesizers are: (1) wideband and fine frequency steps, (2) fast frequency switching time, (3) low phase noise and low spurious level [1]-[3]. A direct frequency synthesizer with a quadrature mixer (QM) driven by a direct digital synthesizer (DDS) [4]-[5] is an effective technique to achieve fine frequency step, fast frequency switching time and low phase noise. A QM suppress image and local leak of single sideband (SSB) mixers in the QM [4]-[5], thus a BPF at output of the direct synthesizer is not required. This implies that bandwidth of the direct synthesizer is equals to the maximum output frequency of the DDS. The maximum output frequency is determined by a DDS clock frequency [6]. Thus to increase bandwidth of the direct synthesizer, the DDS clock frequency has to be increased and DDS consumption current is also increased. Adding an add/subtract circuit in a QM increases bandwidth without increasing a DDS clock frequency [5]. However the extra circuit also consumes current. Moreover a commercial QM IC does not include such a circuit.

In this paper, an approach to increase bandwidth of a direct frequency synthesizer with a QM driven by a DDS without increasing DDS consumption current is presented. The proposed frequency setting algorithm of the DDS that forces to overflow a phase accumulator of the DDS every time period given by the clock frequency. The overflow of the phase accumulator decreases phase of the DDS signal. Typically phase of the DDS signal is only increased. Employing the proposed phase decrement approach that achieves twice frequency bandwidth that given by the maximum DDS output frequency. In the following sections, a configuration of the proposed synthesizer and the frequency setting algorithm is discussed. Measured results of the developed synthesizer are also indicated.

II. CONFIGURATION

A configuration of the direct synthesizer with a QM driven by a DDS is shown in Fig.1. The direct synthesizer consists of a DDS frequency setting circuit, local oscillator (LO), two DDSs, two LPFs and QM. The QM consists of two SSB mixers, 90° phase shifter and adder. The DDS consists of a phase accumulator, ROM and DA converter. ROM saves amplitude data correspond to phase data. The hardware configuration is same as a conventional direct synthesizer [4]. But the frequency setting algorithm of the DDS is different and unique. Details of the algorithm are discussed following sections.

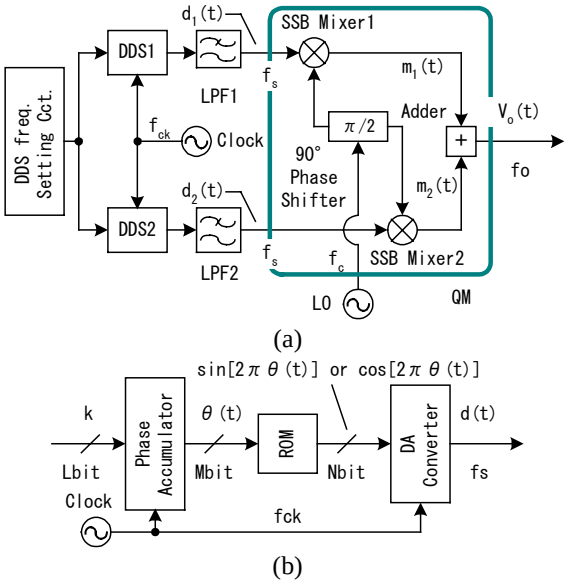

Fig.1. Configuration of the direct synthesizer with a QM driven by a DDS:(a) direct synthesizer, (b) DDS.

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III. Operation Mode of the Synthesizer

A. Phase Increment Mode

In the phase increment mode, output signals of two DDSs $d_1(t)$ and $d_2(t)$ are same as the conventional direct synthesizer [4]-[5], and these are given as follows:

$$\begin{aligned} d_1(t) &= \sin(\omega_s t) \\ d_2(t) &= \cos(\omega_s t) \\ \omega_s &= 2\pi \cdot f_s \end{aligned} \tag{1}$$

$$f_s = k \cdot f_{ck} / 2^L \tag{2}$$

where f_s is the output frequency of the DDS, k is the frequency setting data of the DDS, L is the word length of k, f_{ck} is the DDS clock frequency. DDS with large L is capable to produce fine frequency steps as indicated in (2). Output data of a phase accumulator in the phase increment mode in the case of k=2 and L=3bits is shown in Fig.2. Phase data is incremented with time progress. $d_1(t)$ and $d_2(t)$ are inputted to the QM. Output signals of two SSB mixers of the QM are given as follows:

$$\begin{aligned} m_1(t) &= \sin(\omega_s t) \cdot \cos(\omega_c t) \\ &= 0.5 \cdot \{\sin(\omega_c t + \omega_s t) - \sin(\omega_c t - \omega_s t)\} \\ m_2(t) &= \cos(\omega_s t) \cdot \cos(\omega_c t + \pi/2) \\ &= -0.5 \cdot \{\sin(\omega_c t + \omega_s t) + \sin(\omega_c t - \omega_s t)\} \\ \omega_c &= 2\pi \cdot f_c \end{aligned} \tag{3}$$

where f_c is output frequency of the LO. At output of the QM, two signals $m_1(t)$ and $m_2(t)$ are added by an adder. Finally output signal of the direct synthesizer is given as follows:

$$V_o(t) = m_1(t) + m_2(t) = -\sin(\omega_c t - \omega_s t) \tag{4}$$

(4) indicates that spurious components produced by two SSB mixers are suppressed. Thus no BPF is required at output of the direct synthesizer. The frequency range of the DDS is between DC and the maximum output frequency f_{s_max}. f_{s_max} is given as follows:

$$f_{s\_max} = 0.4 \cdot f_{ck} \tag{5}$$

(4) also indicates that the frequency range of the conventional direct synthesizer [4] and the proposed direct synthesizer in the phase increment mode is between f_c-f_{s_max} and f_c. Thus the bandwidth is f_{s_max}.

B. Phase Decrement Mode

In the phase decrement mode, output signals of two DDSs $d_1(t)$ and $d_2(t)$ are given as follows:

$$\begin{aligned} d_1(t) &= \sin(-\omega_s t) \\ d_2(t) &= \cos(-\omega_s t) \end{aligned} \tag{6}$$

Output data of a phase accumulator in the phase decrement mode in the case of k=2 and L=3bits is shown in Fig.3. Phase data is decremented with time progress. $d_1(t)$ and $d_2(t)$ are inputted to the QM. Output signals of two SSB mixers of the QM are given as follows:

$$\begin{aligned} m_1(t) &= \sin(-\omega_s t) \cdot \cos(\omega_c t) \\ &= 0.5 \cdot \{\sin(\omega_c t - \omega_s t) - \sin(\omega_c t + \omega_s t)\} \\ m_2(t) &= \cos(-\omega_s t) \cdot \cos(\omega_c t + \pi/2) \\ &= -0.5 \cdot \{\sin(\omega_c t - \omega_s t) + \sin(\omega_c t + \omega_s t)\} \end{aligned} \tag{7}$$

Finally output signal of the direct synthesizer is given as follows:

$$V_o(t) = m_1(t) + m_2(t) = -\sin(\omega_c t + \omega_s t) \tag{8}$$

(8) indicates that the frequency range of the proposed direct synthesizer in the phase decrement mode is between f_c and f_c+f_{s_max}. Thus the bandwidth is f_{s_max}.

At the last, (4) and (8) indicates that the bandwidth of the proposed direct synthesizer is twice wider than the conventional direct synthesizer [4] as shown in Fig.4.

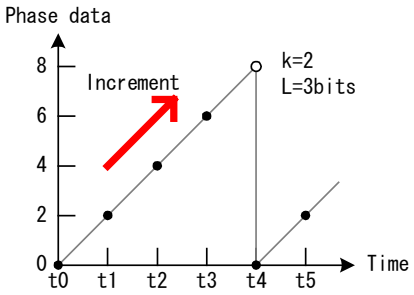

Fig.2. Output data of a phase accumulator in the phase increment mode in the case of k=2 and L=3bits. Phase data is incremented with time progress.

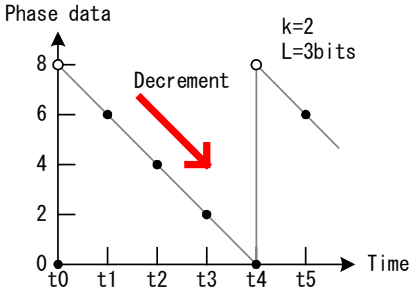

Fig.3. Output data of a phase accumulator in the phase decrement mode in the case of k=2 and L=3bits. Phase data is decremented with time progress.

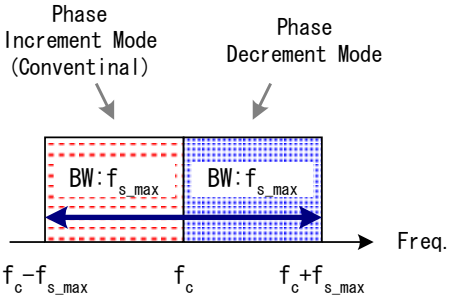

Fig.4. Bandwidth of the direct synthesizer. The proposed direct synthesizer is twice wider than the conventional direct synthesizer.

IV. Phase Decrement by Overflow of the DDS

In general, there is no phase decrement function in a commercial DDS-IC as shown in Fig.3. In this section, phase decrement done by the overflow of the phase accumulator in the DDS is discussed.

A phase accumulator accumulates a frequency setting data k by every time period given by a clock frequency as shown in Fig.2. The accumulated frequency data is a phase data of the DDS output signal. When the phase data $\sigma(t)$ is exceed 2^L then the overflow of the phase accumulator is occurred. In general, k is set to be less than 2^{L-2}, so the overflows does not occurs every time period. New phase data $\sigma'(t)$ after overflow occurred is given as follows:

$$\sigma'(t) = \sigma(t) - 2^L \qquad (9)$$

Now new frequency setting data of the DDS k' is given as follows:

$$k' = 2^L - k \qquad (10)$$

(10) indicates that k' is greater than 2^{L-2}, and overflow occurs every time period. The output data of a phase accumulator employing the overflow technique is shown in Fig.5. As shown in Fig.5, the phase data is decreased as time progress. Thus the phase decrement can be done with a commercial DDS-IC.

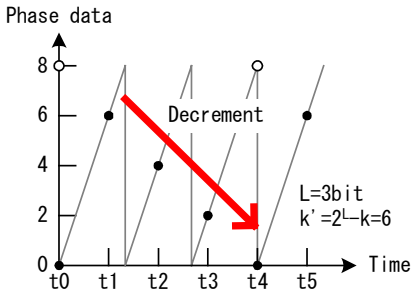

Fig.5. Output data of a phase accumulator employing the overflow technique. The phase data is decreased as time progress.

V. Measured Results

Measured results of the developed synthesizer are shown in Table 1. Analog Device AD9854 (Vcc=3.3V) for a DDS and RF Microdevice RF2422 (Vcc=5V) for a QM are employed for the developed synthesizer. LO frequency f_c is set to be 2GHz-band and clock frequency of the DDS f_{ck} is 300MHz. Thus the maximum DDS output frequency f_{s_max} is 120MHz by (5). Waveform of DDS output signal is shown in Fig.6. Frequency is switched by employing the proposed algorithm. An output spectra of the direct synthesizer is shown in Fig.7. Frequency hopping with the bandwidth of $2f_{s\_max}$ is achieved. Transient characteristic of the direct synthesizer is shown in Fig.8. Frequency switching time is less than 2 μs. Phase noise characteristic of the direct synthesizer is shown in Fig.9. Phase noise is –117dBc/Hz at 100kHz offset. Spurious characteristic of the direct synthesizer is shown in Fig.10. The maximum spurious level is less than –29dBc. Consumption current of the direct synthesizer is shown in Fig.11. Consumption current is 685mA at clock frequency of 300MHz.

Table 1. Measured results of the developed synthesizer.

Parameters	Values
LO frequecy fc	2GHz-band
Clock frequency fck	300MHz
Maximum DDS frequency fs_max	120MHz
Bandwidth at RF output	240MHz
Frequency switching time	2μs
Phase noise at 100kHz offset	-117dBc/Hz
Maximum spurious level	-29dBc
Consumption current	685mA

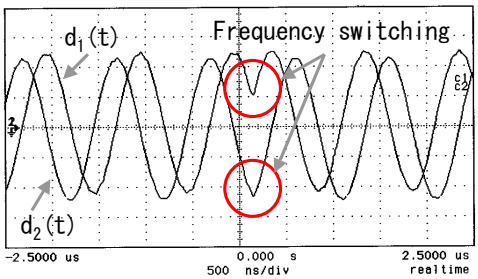

Fig.6. Waveform of DDS output signal. Frequency is switched by employing the proposed algorithm.

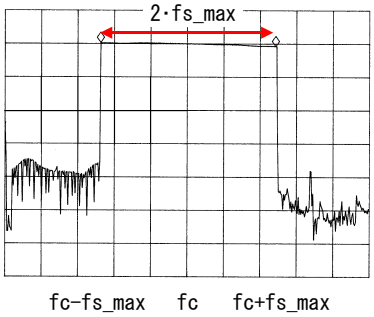

Fig.7. Output spectra of the direct synthesizer. Frequency hopping with the bandwidth of $2f_{s\_max}$ is achieved.

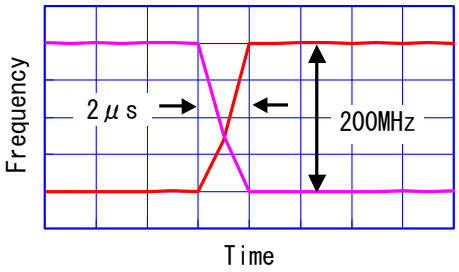

Fig.8. Transient characteristics of the direct synthesizer. Frequency switching time is less than 2 μs.

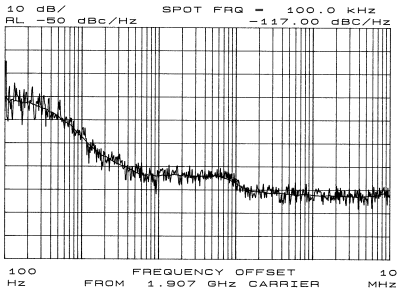

Fig.9. Phase noise characteristics of the direct synthesizer. Phase noise is –117dBc/Hz at 100kHz offset.

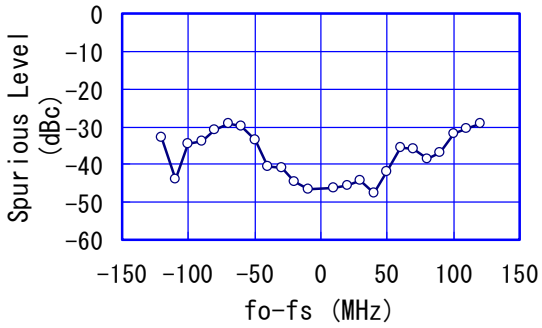

Fig.10. Spurious characteristics of the direct synthesizer. The maximum spurious level is less than –29dBc.

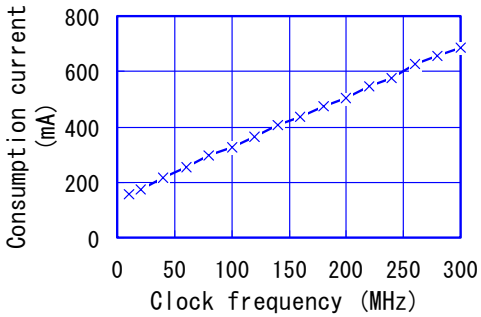

Fig.11. Consumption current of the direct synthesizer. Consumption current is 685mA at clock frequency of 300MHz.

VI. Conclusion

This paper presents a novel approach to increase the bandwidth of the direct frequency synthesizer with a quadrature mixer driven by a DDS. Phase decrement method employing overflow of the DDS phase accumulator is capable to increase bandwidth without increasing consumption current of the DDS and adding an extra circuit. A developed 2GHz-band direct synthesizer achieves 240MHz bandwidth with consumption current of 685mA. Also phase noise of –117dBc/Hz at 100kHz offset and less than 2μs of frequency switching time are achieved.

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